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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,361	07/30/2001	Steven C. Woo	RB1-026US	2536

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EXAMINER	
VERBRUGGE, KEVIN	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/919,361	WOO ET AL.	
	Examiner	Art Unit	
	Kevin Verbrugge	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,24-26,28-35,38-40 and 52-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,24-26,28-35,38-40 and 52-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This final Office action is in response to the amendment filed 7/20/04 by fax which amended almost all pending claims. The amendments and arguments overcome the rejections of record. Claims 1-21, 24-26, 28-35, 38-40, and 52-59 are pending. All rejections and objections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 19, 20, and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,167,484 to Boyer et al.

Regarding claims 19 and 20, Boyer shows the claimed memory controller as system DRAM controller 820 in Fig. 8, for example (a similar circuit is shown in Fig. 9).

He does not explicitly show the claimed refresh logic to refresh the memory cells, however the claimed refresh logic is inherent in his device and its presence in system DRAM controller 820 is indicated by the refresh signal REF leaving controller 820.

He shows the claimed dynamically changeable use registers as tile history qualifiers 808a, 808b, ... 808N. These qualifiers correspond to groups of one or more memory cells, as claimed, and indicate whether the corresponding groups of memory cells are in use (column 5, lines 11-14, column 8, lines 1-3, column 14, line 48 through column 15, line 36, column 24, lines 40-43, column 25, line 50 through column 26, line 25).

Boyer's refresh logic omits refreshing of memory cells that are not in use as claimed (column 5, lines 14-19, column 7, lines 46-51).

Boyer's history qualifiers are not located inside his controller 820.

Boyer's history qualifiers anticipate the claimed recent-access flags, since his history qualifiers are "processed whereby refreshing is not performed on a row of cells that do not need refreshing (i.e., rows that are inactive, or rows that were recently read or written since these accesses inherently do a refresh of the rows)" (emphasis added, column 5, lines 16-19). Boyer clearly teaches that one of the key advantages of his device is keeping track of reads and writes with his history qualifier bits so that memory locations which have recently been read or written (which inherently performs a refresh of the accessed location) are not needlessly refreshed soon after, wasting power and processing time and bandwidth (column 3, lines 22-28). Other passages addressing

this key advantage of his device include column 7, lines 12-18 and 46-51, column 14, lines 38-48, and column 23, lines 3-8.

Regarding claim 24, Boyer variously describes his history qualifiers as referring to rows, refresh groups, pages (column 5, line 13, column 8, line 2, column 10, lines 62-67, column 24, lines 41-43, and column 25, line 65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 7-16, 18, 38, 39, 54-56, 58, and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,167,484 to Boyer et al. in view of U.S. Patent 5,265,231 to Nuwayser.

Regarding claims 1, 2, 11, 12, 38, 54, 56, and 59, Boyer shows the claimed memory controller as system DRAM controller 820 in Fig. 8, for example (a similar circuit is shown in Fig. 9).

He does not explicitly show the claimed refresh logic to refresh the memory cells, however the claimed refresh logic is inherent in his device and its presence in system DRAM controller 820 is indicated by the refresh signal REF leaving controller 820.

He shows the claimed dynamically changeable use registers as tile history qualifiers 808a, 808b, ... 808N. These qualifiers correspond to groups of one or more memory cells, as claimed, and indicate whether the corresponding groups of memory cells are in use (column 5, lines 11-14, column 8, lines 1-3, column 14, line 48 through column 15, line 36, column 24, lines 40-43, column 25, line 50 through column 26, line 25).

Boyer's refresh logic omits refreshing of memory cells that are not in use as claimed (column 5, lines 14-19, column 7, lines 46-51).

Boyer's history qualifiers are not located inside his controller 820.

Nuwayser shows a memory controller 14A in Fig. 1 as 14i in Fig. 2. This memory controller includes DRAM control circuit 23 which includes refresh register circuit 41, detailed in Fig. 3 and discussed at column 6, line 44 through column 7, line 31. Refresh registers 41 include refresh flags for each memory bank controlled by that particular controller.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement Boyer's history decoder 804 (which includes the history qualifiers 808) inside system DRAM controller 820 because Boyer shows the history qualifiers in different locations in different embodiments (in Fig. 8 they are separate from the memory devices while in Fig. 2 they are in the memory devices, as taught at column 14, lines 48-56) clearly indicating that the history qualifiers are not restricted to a single location and furthermore because Nuwayser shows refresh register

flags stored in his memory controller 14i, clearly teaching consolidation of all refresh control circuitry within the memory controller.

Regarding claims 3, 13, 15, 39, 55, and 58, Boyer's history qualifiers anticipate the claimed recent-access flags, since his history qualifiers are "processed whereby refreshing is not performed on a row of cells that do not need refreshing (i.e., rows that are inactive, or rows that were recently read or written since these accesses inherently do a refresh of the rows)" (emphasis added, column 5, lines 16-19). Boyer clearly teaches that one of the key advantages of his device is keeping track of reads and writes with his history qualifier bits so that memory locations which have recently been read or written (which inherently performs a refresh of the accessed location) are not needlessly refreshed soon after, wasting power and processing time and bandwidth (column 3, lines 22-28). Other passages addressing this key advantage of his device include column 7, lines 12-18 and 46-51, column 14, lines 38-48, and column 23, lines 3-8.

Regarding claim 4, Boyer shows plural memory devices in Fig. 8.

Regarding claims 5 and 14, Boyer shows a memory device including the history qualifiers in Fig. 2. In column 14, lines 50-56, he teaches that "the memory system 200 of Fig. 2 ... has history bits located locally within the various memory blocks/tiles and usually in line with the memory row decoder".

Regarding claims 7-10 and 18, Boyer variously describes his history qualifiers as referring to rows, refresh groups, pages (column 5, line 13, column 8, line 2, column 10, lines 62-67, column 24, lines 41-43, and column 25, line 65).

Regarding claim 16, unused memory cells that are not refreshed, as in Boyer's device, are operated at reduced power as claimed (see column 25, lines 60-61 as claimed).

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Claims 25, 26, 29, 30, 31, 52, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,167,484 to Boyer et al.

Regarding claims 25, 26, 52, and 53, Boyer does not explicitly disclose the claimed operating system, however it is inherent in his device as the controlling software running on the processor which is not shown in his figures. Clearly, the processor must have an operating system and it allocates and deallocates memory based on memory mapping portions being active or inactive, as claimed.

Boyer also does not disclose using virtual-to-physical memory mapping, but this was notoriously well-known at the time of the invention as the preferred method of memory management, with the operating system using virtual memory to provide the

processor with a large address space without having to provide the equivalent amount of physical memory. As various virtual pages are needed, they are paged or swapped in and out of the physical memory.

Clearly then, the inactive portions of memory in Boyer's device are not refreshed (see passages cited above including column 26, lines 3-11) and are therefore operated at reduced power.

Regarding claims 29 and 30, Boyer variously describes his history qualifiers as referring to rows, refresh groups, pages (column 5, line 13, column 8, line 2, column 10, lines 62-67, column 24, lines 41-43, and column 25, line 65).

Regarding claim 31, Boyer shows history qualifiers on the memory devices in Fig. 2.

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Claims 28 and 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,167,484 to Boyer et al. in view of Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa.

Regarding claim 28, Boyer does not disclose a cache in his memory controller.

Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a cache in Boyer's memory controller for the improved operation speed provided by a cache as known in the art at the time of the invention. Furthermore, as taught by Ohsawa, data that is cached in the memory controller need not be refreshed in the memory as long as it is eventually written back to the memory.

Regarding claims 32 and 34, Boyer does not disclose a cache in his memory controller.

Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a cache in Boyer's memory controller for the improved operation speed provided by a cache as known in the art at the time of the invention. Furthermore, as taught by Ohsawa, data that is cached in the memory controller need not be refreshed in the memory as long as it is eventually written back to the memory.

Regarding claim 33, Boyer's history qualifiers anticipate the claimed recent-access flags, since his history qualifiers are "processed whereby refreshing is not performed on a row of cells that do not need refreshing (i.e., rows that are inactive, or rows that were recently read or written since these accesses inherently do a refresh of

the rows)" (emphasis added, column 5, lines 16-19). Boyer clearly teaches that one of the key advantages of his device is keeping track of reads and writes with his history qualifier bits so that memory locations which have recently been read or written (which inherently performs a refresh of the accessed location) are not needlessly refreshed soon after, wasting power and processing time and bandwidth (column 3, lines 22-28). Other passages addressing this key advantage of his device include column 7, lines 12-18 and 46-51, column 14, lines 38-48, and column 23, lines 3-8.

Regarding claim 35, Boyer variously describes his history qualifiers as referring to rows, refresh groups, pages (column 5, line 13, column 8, line 2, column 10, lines 62-67, column 24, lines 41-43, and column 25, line 65).

****

Claims 1-21, 24-26, 28-35, 38-40, and 52-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,167,484 to Boyer et al. in view of U.S. Patent 5,265,231 to Nuwayser further in view of Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa.

Regarding claims 6, 17, 21, 40, and 57, Boyer does not disclose a cache in his memory controller.

Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a cache in Boyer's memory controller for the improved operation speed provided by a cache as known in the art at the time of the invention. Furthermore, as taught by Ohsawa, data that is cached in the memory controller need not be refreshed in the memory as long as it is eventually written back to the memory.

Conclusion

Any inquiry concerning a communication from the Examiner should be directed to the Examiner by phone at (703) 308-6663 before 10/14/04 and at (571) 272-4214 after 10/14/04.

Any response to this action should be labeled appropriately (serial number, Art Unit 2188, and After-Final, Official, or Draft) and mailed to Commissioner for Patents, Washington, D.C. 20231 or faxed to (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.

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Art Unit 2188